DHANEKULA INSTITUTE OF ENGINEERING & TECHNOLOGY

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FACULTY PROFILE

Name oftheFaculty	Dr.Gummadi LakshmiMadhumati
Designation	Professor & Head
Date of Joining	15.9.2011
Nature of Association	Regular
Email &PhoneNo	madhumati70@gmail.com&08662583842
Department	Electronics and CommunicationEngineering
Educational Background	1. Ph.D.(ECE) from JNTUH,Hyderabad 2. M.Tech (DSCE) from JNTU,Hyderabad 3. B.E (Electronics) from Shivaji University,Kolhapur
Area of Specialization	Digital Systems and Computer Electronics
ResearchAreas	VLSI Design, Mixed signal VLSI design, Low Power VLSI Design, DSP Architectures and Image processing Architectures, Partial Reconfiguration, System onChip
Experience	26 Years

Sl. No	Institute	Designation	Period
7	Dhanekula Institute of Engineering & Technology	Professor	2011–till date
6	V.R.Siddhartha Engineering College, Vijayawada	Professor	2011–2011
5	Prasad V Potluri Siddhartha Institute of Technology, Kanuru	Professor	2010-2011
4	Prasad V Potluri Siddhartha Institute of Technology, Kanuru	Associate Professor	2007-2010
3	Koneru Lakshmaiah College of Engineering, Greenfields,	Lecturer	2005-2007
2	V.R.Siddhartha Engineering College, Vijayawada	Lecturer	2002-2005
1	V.K.R & V.N.B Polytechnic, Gudivada	Associative lecturer	1993-2001

List of Publications (National andInternationalJournals)

1."Design of CMOS Comparators for FLASH ADC," International Journal of Electronics Engineering (IJEE), Volume 01, Issue 01, 2009,pp. 53-57.

2. "Power and Delay Analysis of a 2–to-1 Multiplexer Implemented in Multiple Logic Styles for Multiplexer-Based Decoder in Flash ADC," International Journal of Recent Trends in Engineering (Electrical and Electronics), Volume 01, Issue 04, 2009,pp. 29-31.

3. "A 0.4V - to - 1.4V Inverter Based 5-bit Flash ADC in 0.18μm CMOS Technology for UWB Applications ," International Journal of Computer Science & Network Security, Volume 09, Issue 06, 2009,pp.255-261.

4."Data Hiding Using EDGE Based Steganography," International Journal of Emerging Technology and Advanced Engineering (IJETAE-2013), Vol. 2, No. 11, November 2012, pp. 285-290.

5. "Edge detection modeling through reconfigurable devices in image processing applications using XPS ," International Conference On Devices, Circuits And Systems – ICDCS 2014,Karunya University, Coimbatore, India.

6."HDL Implementation & Performance Comparison of Various Filtering Techniques Using FPGA," International Journal of Applied Engineering Research, Vol. 9, No. 18, 2014, pp. 5085-5094.

7."Real Time Delay Application for Digital Circuits withPeripheral Based Digital Clock Using FPGA," International Journal of Applied Engineering Research, Vol.9, No.18, 2014, pp. 5115-5123.

8."Reconfigurable Edge detection Processor using Xilinx Platform Studio," International Conference on Devices, Circuits and Systems – ICDCS 2014 March 6-8, 2014, Karunya University, Coimbatore, Tamil Nadu, India, pp. 189-193.

9."Reconfigurable SYSTEM-ON-CHIP design using FPGA." International Conference on Devices, Circuits and Systems – ICDCS 2014, March 6-8, 2014, Karunya University, Coimbatore, Tamil Nadu, India, pp. 70-75.

10."FPGA Implementation of SIFT Algorithm Using Xilinx System Generator," International Conference on Electrical, Electronics, Engineering Trends, Communication, Optimization and Sciences (EEECOS/E3COS)-2014, October 2014, DIET,Ganguru.

11."FPGA Implementation of SIFT Algorithm Using Xilinx System Generator," International Journal of Emerging Trends in Electrical and Electronics (IJETEE – ISSN: 2320-9569), Vol.10, No.10, Oct. 2014, pp. 80-85.

12."FPGA implementation of multi-bit flip-flop based on power optimization technique," International Journal of Applied Engineering Research, Vol.10, No.14,2015, pp. 34042-34046.

13."ASIC Implementation of Low Power NAND Flash Controller With E-MMC Interface,"International Journal of Applied Engineering Research, ISSN: 0973-4562, Vol.10, No.12, 2015, pp. 28779-28793 .

14."Novel Approach of FFT Using CORDIC Algorithm and Analyzed With Chip scope Pro," International Journal of Applied Engineering Research, ISSN: 0973-4562. © Research India Publications, Vol.10, No.10,2015 , pp. 25851-25857.

15."Biometric based industrial machine access control system using FPGA," Journal of Theoretical and Applied Information Technology ISSN: 1992-8645,E-ISSN: 1817-3195, Vol. 79, No.1, 10th September 2015, pp. 76-82 .

16."Implementation and Verification of I²C Single Master Multiple Slave Bus Controller using System Verilog and UVM," International Journal of VLSI System Design and Communication Systems, Management and Research (IJVDCS), Vol.03, Special issuse.08, pages. 1239-1243, October-2015.

17."Dynamically reconfigurable smart traffic system for accident rescue operation,"Journal

of Engineering and Applied Sciences ,Vol.11, No.9, 2016, PP. 1925-1930.

18."IOT based home automation using FPGA,"Journal of Engineering and Applied Sciences , Vol.11, No.9, 2016, PP. 1931-1937.

19."Wireless Secured Data Transmission using Cryptographic Techniques through FPGA," International Journal of Engineering and Technology (IJET), e-ISSN : 0975-4024, p-ISSN : 2319-8613 Vol. 8 No. 1, Feb-Mar 2016, pp. 332-338.

20."Zig Bee Based Wireless Data Transmission with LDPC codes using FPGA," International Journal of Engineering and Technology (IJET), e-ISSN: 0975-4024,p-ISSN : 2319-8613 Vol. 8 No 2 Apr-May 2016 pp. 653-659.

21. "Design of Substantial Delay Block using Voltage Scaled CMOS Inverter and Transmission Gate blend," 2016 International Conference on Microelectronics, Computing and Communications (MicroCom), IEEE Conference Publications: 978-1-4673-6621-2/16/$31.00 ©2016 IEEE, Pages: 1- 6,DOI: 10.1109/MicroCom.2016.7522463

22."FPGA based wireless electronic security system with sensor interface through GSM, "Journal of Theoretical and Applied Information Technology ISSN: 1992-8645,E-ISSN: 1817-3195, Vol.89, Issuse.2, July 2016,pp. 489-494.

23."Design of Dynamically Reconfigurable Input/output Peripheral based Wireless System, "Indian Journal of Science and Technology,ISSN (Print): 0974-6846 ,ISSN (Online) : 0974-5645, Vol. 9, Issue.30, August 2016, pp. 1-9.

24."Low Voltage and Power Efficient Double Tail Comparator with Reduced Delay Time, " International Journal & Magazine of Engineering, Technology, Management and Research, Vol.3, Issue.11, November 2016,ISSN No: 2348-4845, pp. 355-362.

25.FPGA implementation of partially reconfigurable DNA cryptography methods through wireless using ZIGBEE, ARPN Journal of Engineering and Applied Sciences, ISSN : 1819-6608, Vol. 11, Issue.21, November 2016 pp. 12514-12522.

26."Area-Power Efficient Shift Register Using Non-Overlap Delayed Pulsed Clock," International Journal For Technological Research In Engineering Volume 4, Issue. 4, December-2016 ISSN (Online): 2347 – 4718, pp.633-639.

27."FPGA Implementation of DES Algorithm Using DNA Cryptography," Journal of Theoretical and Applied Information Technology, Vol.95. No 10,ISSN: 1992-8645, E-ISSN: 1817-3195 2147, May 2017, pp.2147-2158.

28."Dynamically Evolvable Hardware-Software Co-Design Based Crypto System Through Partial Reconfiguration," Journal of Theoretical and Applied Information Technology, May 2017. Vol.95. No 10, ISSN: 1992-8645, E-ISSN: 1817-3195, pp. 2159 -2169.

29."Stochastic key generation mechanism in Cryptography applications through partial Reconfiguration," Journal of Advanced Research in Dynamical and Control Systems, Vol.9, No.12, September 2017, pp. 1566-1586.

30."PR based DNA cryptosystem design with symmetric and asymmetric cryptography techniques, " Journal of Advanced Research in Dynamical and Control Systems, SP Issue.18, January 2017, PP. 1773-1801.

31."Reconfigurable pseudo biotic key encryption mechanism for cryptography applications," International Journal of Engineering and Technology(UAE),Vol.7, No.15, January 2018, PP. 62-70.

32."FPGA based pseudo random sequence generator using XOR/XNOR for communication cryptography and VLSI testing applications,"International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol.8, No.4, February 2019, PP. 485-494.

33."Triple Notch Reconfigurable Parasitic Monopole Patch Antenna with Defected Ground Structures," International Journal of Microwave and Optical Technology, Vol.15, No.4, July 2020, PP. 318-324.

34.“An Efficient Denoising Architecture of MVD-RCA-SP-FIR filter for Real-time ECG signals,” European Journal of Molecular & Clinical Medicine ,Volume 07, Issue 08, 2020, pp. 1-13, ISSN 2515-8260.

35."An Efficient Denoising Hardware Architecture of CSA-FIR Filter for Real time ECG signals," European Journal of Molecular & Clinical Medicine ,Volume 07, Issue 10, 2020.

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